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Acoustics, Speech, and Signal Processing, 1995. ICASSP-95., 1995 International Conference on , Volume: 4 , 9-12 May 1995
Page(s): 2667 -2670 vol.4

[Abstract] [PDF Full-Text (300 KB)] **IEEE CNF**

2 **Generating synchronous timed descriptions of digital receivers from dynamic data flow system level configuration**
Zepter, P.; Grotker, T.;
European Design and Test Conference, 1994. EDAC, The European Conference on Design Automation. ETC European Test Conference. EUROASIC, The European Event in ASIC Design, Proceedings. , 28 Feb-3 Mar 1994
Page(s): 672

[Abstract] [PDF Full-Text (80 KB)] **IEEE CNF**

3 **PSCP: A scalable parallel ASIP architecture for reactive systems**
Pyttel, A.; Sedlmeier, A.; Veith, C.;
Design, Automation and Test in Europe, 1998., Proceedings , 23-26 Feb 1998
Page(s): 370 -376

[Abstract] [PDF Full-Text (188 KB)] **IEEE CNF**

4 **Performance-driven macro-block placer for architectural evaluation of ASIC designs**
Mosh Nyaga, V.; Mori, Y.; Onodera, H.; Tamaru, K.;
Circuits, Devices and Systems, IEE Proceedings- , Volume: 144
Issue: 3 , Jun 1997
Page(s): 190 -194

[Abstract] [PDF Full-Text (440 KB)] **IEE JNL**

5 **Reusable design of run length coder for image compression application**
Seongmo Park; Inhag Park; Jinjong Cha; Hanjin Cho;
ASICs, 1999. AP-ASIC '99. The First IEEE Asia Pacific Conference on , 1999
Page(s): 274 -277

[Abstract] [PDF Full-Text (276 KB)] **IEEE CNF**

6 **Creating the IC palette [ASIC design]**
Royals, M.; Markas, T.; Tianmaw Yang; Kanopoulos, N.;
Rapid System Prototyping, 1990. 'Shortening the Path from Specification to Prototype'., First International Workshop on , 4-7 Jun 1990
Page(s): 76 -86

[Abstract] [PDF Full-Text (452 KB)] **IEEE CNF**

7 **Practical design assistance at register transfer level using a data path verifier**
Nakamura, H.; Kukimoto, Y.; Fujita, M.; Tanaka, H.;
Computer Design: VLSI in Computers and Processors, 1990. ICCD '90. Proceedings., 1990 IEEE International Conference on , 17-19 Sep 1990
Page(s): 99 -102

[Abstract] [PDF Full-Text (380 KB)] **IEEE CNF**

8 **Automation versus education [chip design process]**
Aleman, E.M.; Soundararajan, K.;
ASIC Conference and Exhibit, 1991. Proceedings., Fourth Annual IEEE International , 23-27 Sep 1991
Page(s): P17 -6/1-4

[Abstract] [PDF Full-Text (276 KB)] **IEEE CNF**

9 **A generalized extraction system for VLSI**
Dukes, M.A.; Brown, F.M.; DeGroat, J.E.;
ASIC Conference and Exhibit, 1991. Proceedings., Fourth Annual IEEE International , 23-27 Sep 1991
Page(s): P4 -8/1-4

[Abstract] [PDF Full-Text (312 KB)] **IEEE CNF**

10 **A 25 MHz 5×7 spatial filter chip for realtime image processing**
Kawata, T.; Son, J.; Tomari, N.; Yamauchi, K.; Miyakawa, N.; Sasuga, K.; Taniuchi, K.;
ASIC Conference and Exhibit, 1991. Proceedings., Fourth Annual IEEE International , 23-27 Sep 1991
Page(s): P3 -1/1-4

[Abstract] [PDF Full-Text (268 KB)] **IEEE CNF**

11 **Using VHDL for modeling and design of processing units**
Navabi, Z.;
ASIC Conference and Exhibit, 1992., Proceedings of Fifth Annual IEEE International , 21-25 Sep 1992
Page(s): 315 -326

[Abstract] [PDF Full-Text (948 KB)] **IEEE CNF**

12 **Interactive register transfer level synthesis using library blocks**
Mignotte, A.; Bertrand, M.-C.; Crastes, M.; Fron, J.; Rampon, J.;
Euro ASIC '92, Proceedings. , 1-5 Jun 1992
Page(s): 53 -58

[Abstract] [PDF Full-Text (480 KB)] **IEEE CNF**

13 **COMET: a set of global transformation algorithms for high-level pipeline synthesis**
Chang, C.-T.; Rose, K.; Walker, R.A.;
VLSI Technology, Systems, and Applications, 1993. Proceedings of Technical Papers. 1993 International Symposium on , 12-14 May 1993
Page(s): 49 -53

[Abstract] [PDF Full-Text (388 KB)] **IEEE CNF**

14 **High-level DSP synthesis using the COMET design system**

Ching-Tang Chang; Rose, K.; Walker, R.A.;
ASIC Conference and Exhibit, 1993. Proceedings., Sixth Annual IEEE International , 27 Sep-1 Oct 1993
Page(s): 408 -411

[Abstract] [PDF Full-Text (320 KB)] **IEEE CNF**

15 **Test design compilers complement top down ASIC design**
Halliday, A.; Young, G.;
AUTOTESTCON '93. IEEE Systems Readiness Technology Conference. Proceedings , 20-23 Sep 1993
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16 **An algorithm for partitioning of application specific systems**

Zebo Peng; Kuchcinski, K.;
Design Automation, 1993, with the European Event in ASIC Design. Proceedings. [4th] European Conference on , 22-25 Feb 1993
Page(s): 316 -321

[Abstract] [PDF Full-Text (536 KB)] **IEEE CNF**

17 **RT-level transformations for gate-level testability**
Bhattacharya, S.; Dey, S.; Brglez, F.;
Design Automation, 1993, with the European Event in ASIC Design. Proceedings. [4th] European Conference on , 22-25 Feb 1993
Page(s): 162 -169

[Abstract] [PDF Full-Text (652 KB)] **IEEE CNF**

18 **Synthesis of self-testable controllers**
Hellebrand, S.; Wunderlich, H.-J.;
European Design and Test Conference, 1994. EDAC, The European Conference on Design Automation. ETC European Test Conference. EUROASIC, The European Event in ASIC Design, Proceedings. , 28 Feb-3 Mar 1994
Page(s): 580 -585

[Abstract] [PDF Full-Text (484 KB)] **IEEE CNF**

19 **A performance-driven macro-block placer for architectural**

evaluation of ASIC designs
Mori, Y.; Moshnyaga, V.G.; Onodera, H.; Tamaru, K.;
ASIC Conference and Exhibit, 1995., Proceedings of the Eighth Annual IEEE International , 18-22 Sep 1995
Page(s): 233 -236

[Abstract] [PDF Full-Text (388 KB)] **IEEE CNF**

20 **Probabilistic resource estimation for pipeline architecture**
Diguet, J.P.; Sentieys, O.; Philippe, J.L.; Martin, E.;
VLSI Signal Processing, VIII, 1995. IEEE Signal Processing Society [Workshop on] , 16-18 Oct 1995
Page(s): 217 -226

[Abstract] [PDF Full-Text (508 KB)] **IEEE CNF**

21 **A methodology for high level synthesis of high performance DSP structures targetting FPGAs**
Shehata, S.; Haroun, B.; Al-Khalili, A.;
ASIC, 1996. 2nd International Conference on , 21-24 Oct 1996
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[Abstract] [PDF Full-Text (328 KB)] **IEEE CNF**

22 **Mapping statechart models onto an FPGA-based ASIP architecture**
Buchenrieder, K.; Pyttel, A.; Veith, C.;
Design Automation Conference, 1996, with EURO-VHDL '96 and Exhibition, Proceedings EURO-DAC '96, European , 16-20 Sep 1996
Page(s): 184 -189

[Abstract] [PDF Full-Text (620 KB)] **IEEE CNF**

23 **Custom ASIC VLSI device for asynchronous transfer mode**
Thomann, M.;
Solid-State Circuits Conference, 1996. Digest of Technical Papers. 43rd ISSCC., 1996 IEEE International , Feb 1996
Page(s): 114 -115, 427

[Abstract] [PDF Full-Text (828 KB)] **IEEE CNF**

24 **Fast prototyping of an ASIC for ATM application using a synthesizable VHDL flexible library**
Claretto, S.; Filippi, E.; Montanaro, A.; Paolini, M.; Turolla, M.;
VHDL International Users' Forum, 1997. Proceedings , 19-22, Oct

1997
Page(s): 88 -94

[Abstract] [PDF Full-Text (588 KB)] **IEEE CNF**

25 **A quadratic programming approach to clock skew scheduling for reduced sensitivity to process parameter variations**
Kourtev, I.S.; Friedman, E.G.;
ASIC/SOC Conference, 1999. Proceedings. Twelfth Annual IEEE International , 1999
Page(s): 210 -215

[Abstract] [PDF Full-Text (364 KB)] **IEEE CNF**

26 **A reconfigurable pipelined IDCT for low-energy video processing**
Suhwan Kim; Ziesler, C.H.; Papaefthymiou, M.C.;
ASIC/SOC Conference, 2000. Proceedings. 13th Annual IEEE International , 2000
Page(s): 13 -17

[Abstract] [PDF Full-Text (416 KB)] **IEEE CNF**

27 **High-level synthesis of nonprogrammable hardware accelerators**
Schreiber, R.; Aditya, S.; Ramakrishna Rau, B.; Kathail, V.; Mahlke, S.; Abraham, S.; Snider, G.;
Application-Specific Systems, Architectures, and Processors, 2000. Proceedings. IEEE International Conference on , 2000
Page(s): 113 -124

[Abstract] [PDF Full-Text (236 KB)] **IEEE CNF**

28 **MetaRTL: raising the abstraction level of RTL design**
Zhu, J.;
Design, Automation and Test in Europe, 2001. Conference and Exhibition 2001. Proceedings , 2001
Page(s): 71 -76

[Abstract] [PDF Full-Text (420 KB)] **IEEE CNF**

29 **Exact AEP model in signature analysis using LCM**
Elsaholy, M.S.;
Computers and Digital Techniques, IEE Proceedings- , Volume: 146

Issue: 5 , Sep 1999
Page(s): 247 -252

[Abstract] [PDF Full-Text (432 KB)] **IEE JNL**

30 **A 3.0 V 40 Mb/s hard disk drive read channel IC**
De Veirman, G.A.; Ueda, S.; Cheng, J.; Tam, S.; Fukahori, K.; Kurisu, M.; Shinozaki, E.;
Solid-State Circuits, IEEE Journal of , Volume: 30 Issue: 7 , Jul 1995
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1 MULTES/IS: an effective and reliable test generation system for partial scan and non-scan synchronous circuits 77%
T. Ogihara , K. Muroi , G. Yonemori , S. Murai
Proceedings of the 1989 26th ACM/IEEE conference on Design automation conference June 1989
This paper describes an automatic test generation system which effectively generates test vectors by recognizing the circuit blocks for which vectors are automatically generated and the circuit blocks for which vectors have to be manually prepared. Test vectors for full scan, partial scan and nonscan synchronous circuit blocks are automatically generated. Test vectors for asynchronous circuit blocks have to be manually prepared.

2 HAL: A multi-paradigm approach to automatic data path synthesis 77%
P. G. Paulin , J. P. Knight , E. F. Girczyc
Papers on Twenty-five years of electronic design automation June 1988

3 Poster session: A four-bit full adder implemented on fast SiGe FPGAs with novel power control scheme 77%
K. Zhou , M. Chu , C. You , J.-R. Guo , J.-R. Guo , J. Mayega , B. S. Goda , R. P. Kraft , J. F. McDonald
Proceedings of the international symposium on Field programmable gate arrays February 2003

The low operating speed of current CMOS Field Programmable Gate Arrays (FPGAs), i.e., 10-220 MHz, has prevented their use in high-speed digital applications. With the advent of IBM Silicon Germanium (SiGe) 7HP technology, designers have been able to design FPGAs operating in the gigahertz range. This paper is going to elaborate on the implementation of a 4-bit ripple-carry full adder (FA) on the new SiGe FPGA with new architectures and a novel power management strategy. The 1-bit FA can be reali ...

4 Poster session: A high resolution diagnosis technique for open and short defects in FPGA interconnects 77%

Mehdi Baradaran Tahoori

Proceedings of the international symposium on Field programmable gate arrays February 2003

A two-step diagnosis flow, coarse-grain and fine-grain, is presented in order to identify a faulty element in the FPGA interconnects. The fault models used for interconnect are open, resistive-open, and bridging fault. The coarse-grain phase identifies the faulty net, the routing between two consecutive sequential elements in the FPGA. This phase is performed by just post-processing tester results for the test configurations used for interconnect testing. During the fine-grain step, the faulty n ...

5 Poster session: Application-dependent testing of FPGAs for bridging faults 77%

Mehdi Baradaran Tahoori

Proceedings of the international symposium on Field programmable gate arrays February 2003

A new technique is presented for testing for bridging faults in the interconnects of an arbitrary design implemented in an FPGA. The configuration of the routing resources used in the original design remains unchanged in the test configurations. Only the logic blocks used in the design are reprogrammed in order to implement single-term functions, logic functions with only one minterm or one maxterm. As shown by formal proofs, all activated faults are detected when single-term functions and appro ...

6 Poster session: A physical retiming algorithm for field programmable gate arrays 77%

Peter Suaris , Dongsheng Wang , Pei-Ning Guo , Nan-Chi Chou

Proceedings of the international symposium on Field programmable gate arrays February 2003

In this paper, we present a physical retiming algorithm for sequential circuits implemented in field programmable gate arrays (FPGAs). This algorithm can speed up the sequential circuits by reducing delay of all

critical paths with negative slacks. By taking advantage of the physical information provided by placed circuits, this algorithm integrates two operations: retiming and register duplication. Retiming moves registers across combinational components. Register duplication moves registers ac ...

7 Poster session: Design strategies and modified descriptions to optimize cipher FPGA implementations: fast and compact results for DES and triple-DES 77%

Gaël Rouvroy , Francois-Xavier Standaert , Jean-Jacques Quisquater , Jean-Didier Legat

Proceedings of the international symposium on Field programmable gate arrays February 2003

We propose a new mathematical DES description that allows optimized implementations. It also provides the best DES and triple-DES FPGA implementations known in term of ratio throughput/area, where area means the number of FPGA slices used. First, we get a less resource consuming unrolled DES implementation that works at data rates of 21.3 Gbps (333 MHz), using VIRTEX II technology. In this design, the plaintext, the key and the mode (encryption/decrytion) can be changed on a cycle-by-cycle basis ...

8 Poster session: Wireless sensor networks: a power-scalable motion estimation IP for hybrid video coding 77%

Federico Quaglio , Maurzio Martina , Fabrizio Vacca , Guido Masera , Andrea Molino , Gianluca Piccinini , Maurizio Zamboni

Proceedings of the international symposium on Field programmable gate arrays February 2003

Wireless Sensor Networks are an emerging phenomenon in the research community. The design and development of network architectures and nodes implementation are fostering many research activities. Due to their wide application fields and pervasive employment possibilities, the investigation of novel classes of wireless sensor nodes is of great concern. In this paper we presented a novel Power-Scalable Motion Estimation IP suitable for video-surveillance over Wireless Sensor Networks. The proposed ...

9 Poster session: Lattice adaptive filter implementation for FPGA 77%

Zdenek Pohl , Rudolf Matoušek , Jirí Kadlec , Milan Tichý , Miroslav Lícko

Proceedings of the international symposium on Field programmable gate arrays February 2003

Our poster introduces an innovative RLS Lattice filter implementation for FPGAs. The signal processing applications typically require wide numeric range, and that poses a problem when using an FPGA implementation. Our approach is based on arithmetic using

logarithmic numeric representation (LNS). The test application - an adaptive noise canceller - has been optimized for the Xilinx Virtex devices. It consumes roughly 70% of all logic resources of the XCV800 device and all block memory cells. The ...

10 Poster session: An FPGA architecture with built-in error correction capability 77%

P. K. Lala , B. Kiran Kumar

Proceedings of the international symposium on Field programmable gate arrays February 2003

The use of very deep submicron technology makes VLSI-based digital systems more susceptible to transient or soft errors, and thus compromises their reliability. This paper proposes an FPGA architecture inspired by the human immune system that allows tolerance of transient errors. The architecture is composed of a two-dimensional array of identical functional cells with different genetic codes. These codes are chosen based on the required functions to be performed by the functional cells. An erro ...

11 Poster session: Synthetic circuit generation using clustering and iteration 77%

Paul D. Kundarewich , Jonathan Rose

Proceedings of the international symposium on Field programmable gate arrays February 2003

The development of next-generation CAD tools and FPGA architectures requires benchmark circuits to experiment with new algorithms and architectures. There has always been a shortage of good public benchmarks for these purposes, and even companies that have access to proprietary customer designs could benefit from designs that meet size and other particular specifications. In this paper, we present a new method of generating realistic synthetic benchmark circuits to help alleviate this shortage. ...

12 Poster session: Reconfigurable randomized K-way graph partitioning 77%

Fatih Kocan

Proceedings of the international symposium on Field programmable gate arrays February 2003

In this paper, a randomized k-way graph partitioning algorithm is mapped onto reconfigurable hardware. The randomized algorithm relies on repetitive running of the same algorithm with different random number sequences to achieve the (near-)optimal solution. The run-time and hardware requirements of this reconfigurable solution per a random number sequence are O(|V|-K) cycles and O(|V|log|V|+|E|) gates and flip-flops, respectively. Performance is

improved further at the expense of more hardware b ...

13 Poster session: An automated and power-aware framework for utilization of IP cores in hardware generated from C descriptions targeting FPGAs 77%

Alex Jones , Prith Banerjee

Proceedings of the international symposium on Field programmable gate arrays February 2003

Use of hand optimized Intellectual Property (IP) logic cores is prolific in hardware design. While IP cores remain a standard way to utilize the improvement in FPGA technology and contend with time to market pressure through reuse, popularity of tools generating hardware descriptions from high-level languages is also increasing in popularity. PACT HDL combines these two methods within a power-aware framework. The PACT HDL compiler generates power optimized VHDL/Verilog from a C language descript ...

14 Poster session: Power-aware architectures and circuits for FPGA-based signal processing 77%

Frank Honoré , Ben Calhoun , Anantha Chandrakasan

Proceedings of the international symposium on Field programmable gate arrays February 2003

This work showcases a power-aware system design methodology for DSP applications on reconfigurable hardware platforms. In particular, an enhanced FPGA architecture is proposed and analyzed for a deep submicron process technology. These enhancements reduce Configurable Logic Block (CLB) usage for distributed arithmetic implementations of signal processing applications by 50% or more thereby reducing the load on interconnect resources. Multi-Threshold CMOS (MTCMOS) circuit design techniques are ag ...

15 Poster session: FPGAs in critical hardware/software systems 77%

Adrian J. Hilton J. Adrian J. Hilton , Gemma Townson , Jon G. Hall

Proceedings of the international symposium on Field programmable gate arrays February 2003

FPGAs are being used in increasingly complex roles in critical systems, interacting with conventional critical software. Established safety standards require rigorous justification of safety and correctness of the conventional software in such systems. Newer standards now make similar requirements for safety-related electronic hardware, such as FPGAs, in these systems. In this paper we examine the current state-of-the-art in programming FPGAs, and their use in conventional (low-criticality) hard ...

16 Poster session: A SC-based novel configurable analog cell 77%
Binlin Guo , Jiarong Tong
Proceedings of the international symposium on Field programmable gate arrays February 2003
This paper presents a high performance Configurable Analog Cell (CAC) which is made up of a Basic Configurable Analog Cell (BCAC) and a digital converter block. The CAC can be used either for Field Programmable Analog Array (FPAA) or for Field Programmable Digital-Analog Mixed Array (FPMA). The BCAC include three innovative Programmable Switch Blocks (PSBs), three Programmable Capacitor Arrays (PCAs), and an amplifier. PSB and PCA can be programmed to generate many equivalent components. In addi ...

17 Poster session: On computation and resource management in an FPGA-based computation environment 77%
Soheil Ghiasi , Karlene Nguyen , Elaheh Bozorgzadeh , Majid Sarrafzadeh
Proceedings of the international symposium on Field programmable gate arrays February 2003
The idea of managing the comprising computations of an application executed in an FPGA-based system is presented. An efficient algorithm for exploiting the timing slack of building blocks of the application is proposed. The slack of these blocks can be utilized by replacing them with slower but "cheaper" modules and by assigning the computations to the proper resources. Thus, our approach manages the comprising computations and system resources at the same time. This is performed without comprom ...

18 Poster session: Testing for bit error rate in FPGA communication interfaces 77%
Yongquan Fan , Zeljko Zilic
Proceedings of the international symposium on Field programmable gate arrays February 2003
FPGAs have witnessed an increased use of dedicated communication interfaces. With their increased use, it is becoming critical to test and properly characterize all such interfaces. Bit error rate (BER) characteristic is one of the basic measures of the performance of any digital communication system. We propose a scheme for BER testing in FPGAs, which exhibits a few orders of magnitude speedup compared to traditional software simulation methods. In this scheme, we include a novel implementation ...

19 Poster session: On hiding latency in reconfigurable systems: the case of merge-sort for an FPGA-based system 77%
Hossam ElGindy , George Ferizis

Proceedings of the international symposium on Field programmable gate arrays February 2003

Recursive solutions are effective software techniques that are difficult to map into hardware due to their dependency on input size and data values. As a result, most high-level design tools do not allow for recursive calls. In this paper we present a technique for mapping the merge-sort algorithm, as a case study, into a reconfigurable system. Our mapping employs an on-line prediction method to reconfigure the necessary hardware only when the need arises, and to hide the reconfiguration delay. ...

20 Poster session: Using FPGAs for data and reorganization engines: preliminary results for spatial pointer-based data structures 77%

Pedro C. Diniz , Joonseok Park

Proceedings of the international symposium on Field programmable gate arrays February 2003

FPGAs have appealing features such as customizable internal and external bandwidth and the ability to exploit vast amounts of fine-grain instruction-level parallelism. In this paper we explore the applicability of these features in using FPGAs as data search and reorganization engines for performing search and reorganization computations over spatial pointer-based data structures for which traditional computing platforms perform poorly. The preliminary experiments, for a set of simple spatial qu ...

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21 Poster session: Recursive circuit clustering for minimum delay and area 77%

Mehrdad Eslami Dehkordi , Stephen D. Brown
Proceedings of the international symposium on Field programmable gate arrays February 2003

We present an effective recursive algorithm for circuit clustering for delay and area minimization, which is applicable to FPGAs. At the highest level of clustering, the circuit is clustered using a modified single-level clustering algorithm. A cluster to netlist transformation technique is proposed, which converts each cluster into a new subcircuit. The algorithm then continues recursively by clustering the generated subcircuits into further levels of clusters. To reduce the amount of node dupl ...

22 Poster session: Track placement: orchestrating routing structures to maximize routability 77%

Katherine Compton , Scott Hauck
Proceedings of the international symposium on Field programmable gate arrays February 2003

The design of a routing channel for an FPGA is a complex process, requiring the careful balance of flexibility with silicon efficiency. With the growing move towards embedding FPGAs into SoC designs, and the opportunity to automatically generate FPGA architectures, this

problem becomes even more critical. The design of a routing channel requires determining the number of routing tracks, the length of the wires in those tracks, and the positioning of the breaks on the tracks. This paper focuses o ...

23 Poster session: Implementation of digital fixed-point approximations to continuous-time IIR filters 77%

J. E. Carletta , R. J. Veillette , F. W. Krach , Z. Fang

Proceedings of the international symposium on Field programmable gate arrays February 2003

An analytical framework for the implementation of digital infinite impulse response filters in fixed-point hardware on FPGAs is presented. It presumes that a continuous-time filter with the desired response is given. Within the framework, the constant coefficient bit widths are determined by accounting for the sensitivity of the filter's pole and zero locations with respect to the coefficient perturbations. The internal signal bit widths are determined by calculating theoretical bounds on the ra ...

24 Poster session: A high-speed successive erasure BCH decoder architecture 77%

Thomas Buerner

Proceedings of the international symposium on Field programmable gate arrays February 2003

A new high speed architecture for a BCH successive erasure decoder is presented. The Berlekamp-Massey based decoder by Sarwate and Shanbhag is extended to handle successive erasures. The critical path in the calculation submodules is increased from Tadd+Tmult to Tadd+Tmult+Tmux. The proposed architecture is implemented exemplary for a BCH(63,45,7) code with up to two erasures on a XILINX Spartan2E300-7. Thus a clock frequency of 95 MHz is reached using 47% of the available slices instead of 105 ...

25 Poster session: Customized regular channel design in FPGAs 77%

Elaheh Bozorgzadeh , Majid Sarrafzadeh

Proceedings of the international symposium on Field programmable gate arrays February 2003

In this paper, we study the problem of customized regular segmentation design in FPGA routing channels. We propose a deterministic algorithm for segmentation design problem in which each interval is assigned to only one segment (1-Segmentation). We solve the problem of maximum number of incremental track assignment of intervals by mincost network flow technique for 1-Segmentation design. The general K-Segmentation design problem can also be solved by some modifications in our algorithm. We have

...

26 Poster session: Design of a fingerprint system using a hardware/software environment 77%

Lee Vanderlei Bonato , Rolf Fredi Molz , João Carlos Furtado , Marcos Flores Ferräo , Fernando G. Moraes

Proceedings of the international symposium on Field programmable gate arrays February 2003

Processing system of fingerprint are CPU time intensive, being normally implemented in software. This paper present a new algorithm for fingerprint features localization, that can be easily implemented in hardware (system-on-a-chip, FPGA). This algorithm is composed by 3 stages, first stage read a fingerprint image (255x255pixels, ash tones) and apply a Gaussian Filter, after this, apply a absolute difference mask (ADM) for detector the edges in the image filtered and the last stage look for fin ...

27 Poster session: A granularity-based classification model for systems-on-a-chip 77%

Stephan Bingemer , Peter Zipf , Manfred Glesner

Proceedings of the international symposium on Field programmable gate arrays February 2003

Field-programmable logic has become an increasingly important technology for the design of digital circuits. One interesting point in the field of reconfigurable logic is its classification within the implementation space of other technologies. Such a classification gains importance if FPGA technology becomes an integral part of Systems-on-a-Chip (SoC). The poster discusses an approach to classify technologies based on their granularity. Therefore, a new distinction into homogeneous and heteroge ...

28 Poster session: An estimation and exploration methodology from system-level specifications: application to FPGAs 77%

Sebastien Bilavarn , Guy Gogniat , Jean Luc Philippe

Proceedings of the international symposium on Field programmable gate arrays February 2003

Rapid evaluation and design space exploration from early specifications are important issues in the design cycle. We propose an original area vs. delay estimation methodology that targets reconfigurable architectures. Two main steps compose the estimation flow: i) structural estimations where architectural solutions are defined at the RT level, this step is technological independent and performs an automatic design space exploration and ii) physical estimations which perform technology mapping t ...

29 Poster session: A single-FPGA implementation of image connected component labelling 77%

K. Benkrid , S. Sukhsawas , D. Crookes , S. Belkacemi

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This paper describes an architecture based on a serial iterative algorithm for Image Connected Component Labelling with a hardware complexity O(N) for an NxN image. The algorithm iteratively scans the input image, performing a recursive non-zero maximum neighbourhood operation. A complete forward pass is followed by an inverse pass in which the image is scanned in reverse order. The process is repeated until no change in the image occurs. The algorithm has been coded in Handel C language and tar ...

30 Poster session: A logic based approach to hardware abstraction 77%

K. Benkrid , S. Belkacemi , D. Crookes

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This paper presents a novel approach to hardware abstraction based on the logic programming language Prolog. This is an attempt to satisfy the dual requirement of abstract hardware design and hardware efficiency. Central to this approach is a hardware description environment called HIDE, which provides more abstract hardware descriptions and compositions than are possible in traditional hardware description languages such as VHDL or Verilog. HIDE enables highly scaleable and parameterised compos ...

31 Poster session: Design framework for the implementation of the 2-D orthogonal discrete wavelet transform on FPGA 77%

A. Benkrid , D. Crookes , K. Benkrid

Proceedings of the international symposium on Field programmable gate arrays February 2003

This paper gives a design framework for the implementation of the 2-D Orthogonal Discrete Wavelet Transform (DWT) on FPGA. The architecture is based on the Pyramid Algorithm Analysis. Our architecture spatially maps the multistage filter banks of the DWT onto the Xilinx Virtex-E FPGA family. In this paper we propose a novel FIR structure to handle the computation along the borders using symmetric extension. The paper includes a new detailed mathematical approach to determine the architecture's d ...

32 Poster session: Making area-performance tradeoffs at the high level using the AccelFPGA compiler for FPGAs 77%

P. Banerjee , V. Saxena , J. Uribe , M. Haldar , A. Nayak , V. Kim , D. Bagchi , S. Pal , N. Tripathi , R. Anderson

Proceedings of the international symposium on Field programmable gate arrays February 2003

Applications such as digital cell phones, 3G wireless receivers, and voice over IP, require DSP functions that are typically mapped onto general purpose DSP processors. With the introduction of advanced FPGA architectures which provide built-in DSP support such as the Xilinx Virtex-II, and the Altera Stratix, a new hardware alternative is available for DSP designers. DSP design has traditionally been divided into algorithm development and hardware/software implementation. The majority of DSP alg ...

33 Poster session: FPGA implementation of a fast Hadamard transformer for WCDMA 77%

Sanat Kamal Bahl , Jim Plusquellic

Proceedings of the international symposium on Field programmable gate arrays February 2003

In code division multiple access (CDMA) systems the base station identifies each user in a cell by unique orthogonal (Walsh) codes. The Walsh codes are generated at the transmitter using a Walsh-Hadamard function. A Fast Hadamard Transformer (FHT) is used at the receiver to decode the transmitted codes. The purpose of this study is to design a FHT which utilizes less hardware resources as compared to the existing designs and also suggest means for reducing the input length of the Walsh sequence. ...

34 Poster session: FPGA-based design of an evolutionary controller for collision-free robot navigation 77%

M. A. H. B. Azhar , K. R. Dimond

Proceedings of the international symposium on Field programmable gate arrays February 2003

The employment of field programmable gate arrays (FPGAs) to a robot controller is very attractive, since it allows for fast IC prototyping and low cost modifications. The speedup is achieved because of pipelining and dedicated functions in hardware that are customized to the problem. The self learning ability and the adaptive nature of an Artificial Neural Network (ANN) makes it a good candidate for the control structure of a robot's navigation. An evolutionary approach in designing robots can e ...

35 Special session on on-chip multi-processing: Design experience of a chip multiprocessor merlot and expectation to functional verification 77%

Satoshi Matsushita

Proceedings of the 15th international symposium on System Synthesis October 2002

We have fabricated a Chip Multiprocessor prototype code-named Merlot to proof our novel speculative multithreading architecture. On Merlot, multiple threads provide wider issue window beyond ordinal instruction level parallel (ILP) processors like superscalar or VLIW. With the architecture, we estimate 3.0 times speedup against single processing elements (PE) on speech recognition code and IDCT code with four PEs. Merlot integrates on-chip devices, PCI interface, and SDRAM interfaces. We have en ...

36 Delivering acceleration: the potential for increased HPC application performance using reconfigurable logic 77%

David Caliga , David Peter Barker

Proceedings of the 2001 ACM/IEEE conference on Supercomputing (CDROM) November 2001

SRC Computers, Inc. has integrated adaptive computing into its SRC-6 high-end server, incorporating reconfigurable processors as peers to the microprocessors. Performance improvements resulting from reconfigurable computing can provide orders of magnitude speedups for a wide variety of algorithms. Reconfigurable logic in Field Programmable Gate Arrays (FPGAs) has shown great advantage to date in special purpose applications and specialty hardware. SRC Computers is working to bring this technolog ...

37 Embedded software automation: from specification to binary: Retargetable binary utilities 77%

Maghsoud Abbaspour , Jianwen Zhu

Proceedings of the 39th conference on Design automation June 2002

Since software is playing an increasingly important role in system-on-chip, retargetable compilation has been an active research area in the last few years. However, the retargetting of equally important downstream system tools, such as assemblers, linkers and debuggers, has either been ignored, or falls short of meeting the requirements of modern programming languages and operating systems. In this paper, we present techniques that can automatically retarget the GNU binutils tool kit, which con ...

38 Constructing and exploiting linear schedules with prescribed parallelism 77%

Alain Darte , Robert Schreiber , B. Ramakrishna Rau , Frédéric Vivien

ACM Transactions on Design Automation of Electronic Systems (TODAES) January 2002

Volume 7 Issue 1

We present two new results of importance in code generation for and synthesis of synchronously scheduled parallel processor arrays and multicluster VLIWs. The first is a new practical method for

constructing a linear schedule for the iterations of a loop nest that schedules precisely one iteration per cycle on each of a prescribed set of processors. While this problem goes back to the era in which systolic computation was in vogue, it has defied practical solution until now. We provide a closed ...

39 IP Design and Reuse: High-level automatic pipelining for sequential circuits 77%

Maria-Cristina V. Marinescu , Martin Rinard

Proceedings of the international symposium on Systems synthesis - Volume 14 September 2001

This paper presents a new approach for automatically pipelining sequential circuits. The approach repeatedly extracts a computation from the critical path, moves it into a new stage, then uses speculation to generate a stream of values that keep the pipeline full. The newly generated circuit retains enough state to recover from incorrect speculations by flushing the incorrect values from the pipeline, restoring the correct state, then restarting the computation.We also implement two extensions t ...

40 Architecture Analysis and Automation: Automatic layout of domain-specific reconfigurable subsystems for system-on-a-chip 77%

Shawn Phillips , Scott Hauck

Tenth ACM International Symposium on Field-Programmable Gate Arrays February 2002

When designing SOCs, a unique opportunity exists to generate custom FPGA architectures that are specific to the application domain in which the device will be used. The inclusion of such a device will provide an efficient compromise between the flexibility of software and the performance of hardware, while at the same time allowing for post-fabrication modification of circuits. To automate the layout of reconfigurable subsystems for system-on -a-chip we present template reduction, standard cell, ...

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ACM Transactions on Design Automation of Electronic Systems (TODAES) April 2001
Volume 6 Issue 2
We present a survey of the state-of-the-art techniques used in performing data and memory-related optimizations in embedded systems. The optimizations are targeted directly or indirectly at the memory subsystem, and impact one or more out of three important cost metrics: area, performance, and power dissipation of the resulting implementation. We first examine architecture-independent optimizations in the form of code transoformations. We next cover a broad spectrum of optimizati ...

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Reiner Hartenstein
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The paper gives a brief survey over a decade of R&D on coarse grain reconfigurable hardware and related compilation techniques and points out its significance to the emerging discipline of reconfigurable computing.

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P. G. Paulin , J. P. Knight , E. F. Girczyc
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This paper discusses the gate-level automatic test pattern generation (ATPG) methods and techniques for sequential circuits. The basic concepts, examples, advantages, and limitations of representative methods are reviewed in detail. The relationship between gate-level sequential circuit ATPG and the partial scan design is also discussed.

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... **ASIC** de- velopment, despite resulting in highly eAEcient designs ... area and power consumption for **register** files of ... A number of approaches to **ASIP** design where ...
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... Processor. **ASIC**. Memory. ... where N is the no. of Functional Units connected to the **register** file. ... Current **ASIP** vendors do not offer customizable interconnects. ...
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... coprocessors, access to the same **register** set as reg ... the software (in form of FPGA or **ASIC** coprocessor) has ... the multi-processor framework for **ASIP** generation as ...
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... with BSS Behavioural **Specification** Processing unit ... non utilisées * Processeurs dédiés (**ASIC**) performants mais ... programmables " maison " **ASIP** (DSP ou ...
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... without the use of CKFs and **register** arrays. ... of an industrial C compiler for an **ASIP**
used in ... com, 2000 [2] Austria Mikro Systeme International:**asic**.amsint.com ...
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[PPT] Introduction
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... System-on-a-chip. Peripherals. **ASIP** or. Processor. Core. RAM. ... System. evaluation.
An **ASIC** design methodology. Logic synthesis. **Register**-transfer-level. description. ...
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... u u With With higher higher - - design volume design volume to compensate for higher to compensate for higher NREs NREs u u From **ASIC** to From **ASIC** to **ASIP ASIP** ...
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... unit size, **register** size, multiplexer size, state-**register** size, control ... the selection of resources, which includes processor, **ASIC**, memory, **ASIP**, DSP etc ...
research.cs.tamu.edu/codesign/rts1.pdf - Similar pages

[PPT] 1999 **ASIC** Conference FP1.3
File Format: Microsoft Powerpoint 97 - View as HTML
... Higher performance, lower power than commercial cores, more flexibility than **ASIC**. ... **ASIP** Design Flow. ... Instruction selection, scheduling, and **register** allocation. ...
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[PDF] **ASIP** Design Methodology for telecommunications
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... Using a large shifter **register**, the co-processor handles ... Protocol Processor) from [7] is an **ASIC** controlled by a ... some key points for the **ASIP** architecture are ...

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... model (=RC) Gate level model 1/0/X/U (ns) **Register**-transfer level ... MPU running application/OS) - - Designer programmable (Dedicated MPU, **ASIP**, DSP) Designer ...
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... auf 100 mm 2 Silizium DSP: TMS320C6713 DSP **ASIC ASIC**: 50 Mil ... FPGA FPGA: 500.000 Gatter **ASIP ASIP**: 40 Mil ... Floorplan Transistoren Gatter Module (**Register**, ALUs, MUX ...
wwwhni.uni-paderborn.de/sct/lehre/ems/material/ download.php3?dl=EMS-Folien_01.pdf - Similar pages

Sharad Malik
... **Register** Transfer Level Synthesis: From Theory to Practice", IEEE International Conference on VLSI Design, January 1996. ... From **ASIC** to **ASIP**: The Next ...
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... **ASIC** models ... generated automatically from description of processor " From **register**
description and instruction set (behavior) " From structure of **ASIP** data path ...
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[PPT]Embedded Systems
File Format: Microsoft Powerpoint 97 - View as HTML
... **ASIC** models. Gate. ... From **register** description and instruction set (behavior). From
structure of **ASIP** data path as generated by high level synthesis (structure).
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[PDF]Microsoft PowerPoint - SoC_16_Compiler_ASIP_Challenge-1028.ppt
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... on volume of product MetaCore (**ASIP**) General-purpose processor **ASIC** MetaCore development ... 1997
Risc-like Micro-architecture (**register** based operation ...
sonata.kaist.ac.kr/course/ee878-2002/lecture/ SoC_17-Compiler_ASIP_Challenge-1028.pdf - Similar pages

[PDF]Architecture Selection
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... med . high high order of magnitude order of magnitude **ASIC** FPGA **ASIP** GP proc. ... Fö
8- 14 Specialization of a VLIW **ASIP** Crossbar / Bus **Register** File 3 ...
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ballade.cs.ucla.edu/~kohcc/sigdacdrom/eurdac96/papers/ 1996/eurdac96/htmfiles/sun_sgi/frames/eurai.htm - 62k - Cached - Similar pages

[PDF]System Value and Cost
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... Level * Algorithmic Level * **Register**-Transfer Level ... Electronic Design Automation **ASIC** - Application Specific Integrated Circuit **ASIP** - Application Specific ...
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... Requirements **ASIC ASIP**: Tool Requirements Key aspects: Key aspects: Ability to specify

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... coprocessors, access to the same **register** set as reg ... the software (in form of FPGA or **ASIC** coprocessor) has ... the multi-processor framework for **ASIP** generation as ...
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... model 1/0/X/U (ns) **Register**-transfer level ... Heterogeneous Hardware : Specific hardware (DSP, MCU **ASIC**, IP, Memory ... hand coded SW (Dedicated CPU, **ASIP**, DSP) SW ...
tima.imag.fr/MPSOC/2002/slides/MPSOC_02aaj.pdf - Similar pages

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File Format: PDF/Adobe Acrobat - View as HTML
... ORZ compilation compilation **Specification** partitioning partitioning ... controllers, DSP's, **ASIP's**, **ASIC's**, FPGA's, etc ... elements: memories, **register** files, registers ...
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... discusses the VHDL language supports for the delay and concurrency, algorithmic
modeling and **register**-transfer-level ... 디지탈 **ASIC** 및 **ASIP** 설계 (**ASIC** ...
vada.skku.ac.kr/Intro/grad-course.html - 32k - Cached - Similar pages

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... Higher performance, lower power than commercial cores, more flexibility than **ASIC**. ... **ASIP**
Design Flow. ... Detailed **register** allocation with varying load/ spill costs. ...
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... with BSS Behavioural **Specification** Processing unit ... non utilisées * Processeurs dédiés
(**ASIC**) performants mais ... programmables "maison" **ASIP** (DSP ou ...
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File Format: Microsoft Powerpoint 97 - View as HTML
... FPGA. **ASIC**. Estimation of: Clock. ... Performance analysis for the. **ASIP** parameter,. number of **register** windows. ASSET/ ASSIST presentation August 2, 2002. Outline. 27. ...
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[PPT]Overview

File Format: Microsoft Powerpoint 97 - View as HTML
... Processor. **ASIC**. Memory. ... Current **ASIP** vendors do not offer customizable interconnects. Instruction encoding and decoding: ... RF1. RF2. **Register** Files. Functional Units. ...
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